Notice of Allowability	Application No.	Applicant(s)	
	09/739,956	PETHER ET AL.	
	Examiner	Art Unit	
	Kimbinh T. Nguyen	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communication filed 11/17/04*.

2. ☒ The allowed claim(s) is/are *1,4-11,13-15,19,20 and 23-30*.

3. ☒ The drawings filed on *19 December 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *3/18/05* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Christopher Maiorana on 03/18/05.

The application has been amended as follows:

Claim 1. (Currently amended) An apparatus for generating a region of graphics on a display, the apparatus comprising:

a bus having a first address range and a second address range;

a plurality of registers within said first address range configured to store an X coordinate and a Y coordinate of a pixel to be drawn on said display;

a memory directly connected to said bus and responsive within said second address range;

a calculation circuit configured to calculate an address in said second address range for storage of data corresponding to said pixel in dependence on said X and said Y coordinates;

a control circuit configured to control writing of said data in said memory across said bus by driving said address onto said bus; and

a clipping circuit for (i) comparing said x and said Y coordinates with predetermined clipping limits and (ii) generating a clipping signal configured to indicate that at least one of said X and said Y coordinates falls outside said predetermined clipping limits; wherein (i) a first register of said registers is memory mapped to a first location and a second location in said first address range and (ii) a second register of said registers is memory mapped to a third location and a fourth location in said first address range.

Claim 4. (Currently amended) The apparatus as claimed in claim (3) 1, wherein said control circuit is further configured to inhibit writing of said data to said address in response to said clipping signal.

Claim 5. (Currently amended) The apparatus as claimed in claim (3) 1 wherein said control circuit is further configured to prevent calculation of said address in response to said clipping signal.

Claim 6. (Currently amended) The apparatus as claimed in claim (3) 1, wherein said data is discarded when at least one of said X and said Y coordinates fall outside said predetermined clipping limits.

Claim 7. (Canceled).

Claim 8. (Currently amended) The apparatus as claimed in claim (7) 1, wherein said apparatus further comprises: an address decoder for (i) monitoring said first, said second, said third and said fourth (memory) locations and (ii) applying a location signal to said control circuit representative of an address location being written to.

Claim 15. (Currently amended) An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register accessible via a bus for storing coordinates of a pixel to be dawn on said display;

a calculation circuit for calculating an address in a memory directly connected to said bus for storage of data corresponding to said pixel in response to said coordinates; (and)

a control circuit for controlling said register and said calculation circuit to cause said data to be stored in said memory across said bus by driving said address onto said bus, wherein said calculation circuit is configured to output said address in a first part and a second part, said first part comprising a word address corresponding to said address in said memory and representing a single memory word and said second part comprising a bit address representing a position of said pixel data within said single memory word (.) ;

a second register for storing said pixel data in said single memory word prior to said single memory word being written to said address in said memory;

a logic unit for writing data to said second register in dependence on said address calculated by said calculation circuit, wherein said logic unit combines data for at least two pixels to be drawn in dependence on said address of each of said pixel to permit storage of said data for said pixels in said single memory word; and

a comparator connected to said calculation circuit for (i) receiving said addresses, (ii) comparing said addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if said addresses are identical.

Claim 16 (Canceled).

Claim 17 (Canceled).

Claim 18 (Canceled).

Claim 19. (Currently amended) The apparatus as claimed in claim (18) 15, wherein said control circuit is further configured to combine said data for said pixels in response to a receipt of said same address signal.

Claim 20. (Currently amended) A method of generating a region of graphics on a display, the method comprising:

(A) storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

(B) storing a Y coordinate for said pixel in said first address range;

(C) calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependence on said X and said Y coordinates;

(D) controlling writing of said data across said bus into a memory directly connected to said bus by driving said address onto said bus; and

(E) memory mapping a first register storing said X coordinate to a first location and a second location in said first address range; (and)

(F) memory mapping a second register storing said Y coordinate to a third location and a fourth location in said first address range;

(G) comparing said X and said Y coordinates with predetermined clipping limits; and

(H) discarding said pixel data in response to at least one of said X and said Y coordinates exceeding said predetermined clipping limits.

Claim 21. (Canceled)

Claim 23. (Currently amended) The method as claimed in claim (22) 20, further comprising:

monitoring said first, said second, said third and said fourth locations for a write.

Claim 30. (Currently amended) An apparatus for generating a region of graphics on a display, the apparatus comprising:

means for storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

means for storing a Y coordinate for said pixel in said first address range,

means for calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependence on said X and said Y coordinates; (and)

means for controlling writing of said data across said bus into a memory directly connected to said bus by driving said address onto said bus;

means for (i) memory mapping a first register storing said x coordinate to a first location and a second location in said first address range and (ii) memory mapping a second register storing said y coordinate to a third location and a fourth location in said first address range;

means for comparing said x and said y coordinates with predetermined clipping limits; and

means for discarding said x and y coordinates exceeding said predetermined clipping limits.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

Claim 1, the prior art does not teach a calculation circuit configured to calculate an address in said second address range for storage of data corresponding to the pixel in dependence on said X and said Y coordinates; a control circuit configured to control writing of the data in the memory across the bus by driving said address onto the bus; a first register of said registers is memory mapped to a first location and a second location in said first address range and (ii) a second register of said registers is memory mapped to a third location and a fourth location in said first address range.

Claim 15, the prior art does not teach a logic unit for writing data to the second register in dependence on said address calculated by said calculation circuit, wherein said logic unit combines data for at least two pixels to be drawn in dependence on said address of each of said pixel to permit storage of said data for said pixels in said single memory word; and a comparator connected to said calculation circuit for (i) receiving said addresses, (ii) comparing said addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if said addresses are identical.

Claim 20, the prior art does not teach controlling writing of said data across said bus into a memory directly connected to said bus by driving said address onto said bus; and memory mapping a first register storing said X coordinate to a first location and a second location in said first address range; memory mapping a second register storing said Y coordinate to a third location and a fourth location in said first address range.

Claim 30, the prior art does not teach calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependence on said X and said Y coordinates; controlling writing of said data across said bus into a memory directly connected to said bus by driving said address onto said bus.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimbinh T. Nguyen whose telephone number is (571) 272-7644. The examiner can normally be reached on Monday to Thursday from 7:00 AM to 4:30 PM. The examiner can also be reached on alternate Friday from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman, can be reached at (571) 272-7653. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 18, 2005

KIMBINH T. NGUYEN
PRIMARY EXAMINER